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EXAMINER	
ROSARIO-VASQUEZ, DENNIS	

ART UNIT	PAPER NUMBER
2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,011	RATCLIFFE, MARTIN J.	
	Examiner	Art Unit	
	Dennis Rosario-Vasquez	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amend A. 06/01/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment was received on June 1, 2004 and has been entered and made of record. Currently, claims 1-23 are pending.

Specification

2. The amendment to the specification has been reviewed and is acceptable.

Response to Arguments

3. Applicant's arguments, see Amend A, pages 11,12, filed June 1,2004, with respect to the rejection(s)of claim(s) 1,15, and 16 under Malinowski et al. (US Patent 5,574,572 A) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shirota (US Patent 4,376,290 A).

4. Applicant's arguments, see Amed. A, page 13 filed June 1, 2004, with respect to the rejection(s)of claim(s) 9 under Malinowski in view of Chen et al. (US Patent 6,356,315 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shirota.

5. Applicant's arguments, see Amend. A, page 13 filed June 1, 2004, with respect to the rejection(s)of claim(s) 10 under Malinowski et al. in view of Chen et al. in further view of Fandrianto et al. (US Patent 5,982,459 A) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shirota.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 21 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 21 and 22, lines 3 and 4 contains the phrase "(ii) a BTMP after luma state, (iii) an SPU/VBI state". Support and a description for the above phrase in the specification were not found. The only support of the above phrase was found on page 30, line 7, which did not provide enough details as for the scope of claims 21 and 22.

Claim Objections

8. The following quotations of 37 CFR § 1.75(a) is the basis of objection:

> (a) The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

9. Claim 1 is objected to under 37 CFR § 1.75(a) as failing to particularly point out and distinctly claim the subject matter which the applicant regards as his invention or discovery.

Claim 1, line 13 has the word "generated" which ought to be amended to "generator".

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1,2,3,4,6,7,8,9,11,12,13,14,15,16,17,18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) in view of Shirota (US Patent 4,376,290 A).

Regarding claim 1, Malinowski et al. teaches an apparatus for variably scaling video picture signals comprising:

a) a first circuit (fig. 6, numerals 52 and 54 located on the left side of figure 6) configured to generate one or more data signals (The outputs 52 and 54 on the left side of fig. 6.) vertically scaled to a first value ("order of vertical...scaling" at Makinowski et al., col. 6 line 62 and 52 and 54 perform vertical processing as shown in fig. 6.) in response to (i) said video picture signals (Y and U,V inputs of fig. 6) and (ii) one or more first control signals (K_v is a first vertical scaling factor in 52 on the left side because it is predetermined as mentioned in col. 3, line 47, col. 6, lines 19,20 and from col. 6, line 58 to col. 7, line 2.);

b) a second circuit (fig. 6, numerals 52 and 54 located on the right side of figure 6.) configured to generate one or more output signals (Y and U,V outputs of fig, 6) horizontally scaled to a second value ("order of... horizontal scaling" at Malinowski et al. , col. 6 line 62 and 52 and 54 on the left side perform horizontal processing as shown in fig. 6.) in response to (i) said one or more data signals (Y and U,V inputs of fig. 6) and (ii) said one or more first control signals (Figure 6, numerals 52 and 54 on the right side of figure 6 have the same characteristics of numerals 52 and 54 located on the right side of figure 6 except for a horizontal scaling factor of K_h as mentioned in col. 6, lines 19,20 and from col. 6, line 58 to col. 7, line 2. K_h is also a first control signal because it is predetermined as mentioned in col. 3, line 47.), wherein said first value and said second value are independently selectable (Malinowski et al. states," the vertical and horizontal scaling factors may be independent (col. 7 lines 1,2).").

Malinowski et al. does not teach the remaining limitation of an address generator circuit configured to generate said one or more first control signals. However, Malinowski does suggest using different values of a control signal as mentioned in col. 1, line 54 and col. 3, lines 47 and 64.

However, Shirota teaches the remaining limitation of an address generator circuit (fig. 13, num. 70) configured to generate said one or more first control signals (fig. 13, labels CT_3 to CT_6 , CT_A, CT_B , $CT_{,1,2,7,8}$), wherein said address generator comprises a finite state machine (a group of logic gates 78-89 of fig. 13 that produce finite outputs of one or zero.) configured to allow mulitiple luma and multiple chroma picture requests ($(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$ for a luma picture "read request" and $(SL_n)_c$ and $-(SL_n)_c$ for a chroma picture "read request" of fig. 13 as mentioned in col. 19, lines 57-65 and col. 20, lines 36-39.) to follow in sequence (This portion of the limitation was addressed in claim 15.)

The group of logic gates 78-89 of fig. 13 that correspond to the claimed finite state machine are configured to generate the control signals CT_3 to CT_6 , CT_A, CT_B , $CT_{,1,2,7,8}$ of fig. 13 upon a read request signal 76 and 77 of fig. 13 and mentioned in col. 19, lines 57-64 and col. 21, lines 31-36 that request the mulitiple luma and chroma picture requests in a sequence as discussed in claim 15.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Malinowski et al.'s teaching of an interpolator 52 of fig. 6 with a scaling factor K as the claimed control signal with Shirota's teaching of a control circuit 70 and associated luma and chroma output control signals CT_A , CT_B , $CT_{1,2,7,8}$, CT_3 , CT_4, CT_5 , CT_6 of fig. 13 that correspond with the claimed control signal, because the luminance component or picture request, $(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$, will be free at all times of spatial deviation with respect to a line in col. 20, lines 31-33.

Regarding claim 2, Makinowski et al. discloses the apparatus according to claim 1, wherein said first circuit comprises (i) a luma circuit (The upper half portion above the dashed line of 52 and 54 on the left side of fig. 6) configured to generate a luma component (fig. 6, label "Y" is luminance component that is outputted from the upper half of 52 and 54 on the left side of fig. 6.) of said data signals (The upper outputs 52 and 54 on the left side of fig. 6.) and (ii) a chroma circuit (The lower half of numerals 52 and 54 of fig. 6) configured to generate one or more chroma components of said data signals (fig. 6, label "U,V" is a chrominance signal that is outputted from the lower half of 52 and 54 of fig. 6). Makinowski et al. states," With reference to FIG. 6, color video input may be separated into Y and UV components and provided to staged interpolators 52 and filters 54...(col. 6 lines 59-62).") Therefore either interpolator 52 or filter 54 can function as a luma circuit or chroma circuit.

Regarding claim 3, Makinowski et al. discloses the apparatus and method according to claims 1 and 16, wherein said second circuit is further configured to decimate (fig. 6, num. 54 or fig. 4 and fig. 5, numeral 40 are like parts at col. 6, lines 32 and 66) on the right side of figure 6 is a decimator and interpolate (fig. 6, num. 52 is an interpolator on the right side of figure 6) said data signals.

Regarding claim 4, Makinowski et al. discloses the apparatus according to claim 1, wherein said apparatus is programmable ("process of positioning the U and V outputs" using hardware at col. line. 8 ,lines 10,11) to scale said output signals to one or more display modes (Multiple display formats (4:2:2 and 4:2:0 output formats) are mentioned in col. 8 lines 35-38.).

Regarding claim 6, regarding claim 6, Makinowski et al. teaches the apparatus according to claim 4, wherein said one or more output signals (Y and U,V outputs of fig. 6.) are scalable to any value in a range of 0.25 times to 4.0 times (The output signals can be scaled from a range "between one and two" for a "special case" as mentioned in col. 6 ,lines 26, 32-34.) said video picture signals (Y and U,V inputs of fig. 6).

Regarding claim 7, Makinowski et al. teaches the apparatus according to claim 2, wherein said luma circuit (The upper half of 52 and 54 on the left side of fig. 6.) comprises:

a first memory circuit (Figure 2, num. 22 is a buffer located within figure 6, numeral 52 on the left hand side.) configured to buffer a luma component (Y input component of fig. 6.) of said video picture signals (Y and U,V inputs of fig. 6);

a first filter circuit (fig. 6, numeral 54 on the left side of figure 6.) coupled to said first memory circuit (Figure 2, num. 22 is a buffer located within figure 6, numeral 52 on the left hand side.) and configured to generate said data signals (The upper outputs 52 and 54 on the left side of fig. 6.);

and a second memory circuit (Figure 2, num. 22 is a buffer located within figure 6, numeral 52 on the right hand side.) coupled to said first filter circuit (fig. 6, numeral 54 on the left side of figure 6.) and configured to buffer said luma component (Y input component of fig. 6.) of said data signals (Y and U,V inputs of fig. 6).

The second memory circuit is configured to buffer the Y input component after the second memory circuit and associated filter outputs the Y input component.

Claim 8 is similar to claim 7, except for requiring a chroma circuit that is shown as the bottom half of 52 and 54 of fig. 6.

Regarding claim 9, Shirota teaches the apparatus according to claim 1, wherein said generator circuit (Shirota, fig. 13, num. 70) is configured to generate said control signals (fig. 13, labels CT_3 to CT_6, CT_A, CT_B, $CT_{,1,2,7,8}$) in response to one or more second control signals (Fig. 13, num. 77 and 76) from a microcontroller circuit (fig. 2, num 33).

The second control signals 76 and 77 are "request signals" of fig. 13 that are generated from the circuit of fig. 2, num 33 as mentioned in col. 9, lines 36-40.

Regarding claim 11, Makinowski et al. discloses the apparatus according to claim 7, wherein said first filter circuit (fig. 6, numeral 54 on the left side of figure 6.) further comprises a first accumulator circuit (Fig. 4, num. 44 is an accumulator as mentioned in col. 5 , lines 1,2 within fig. 6, numeral 54 on the left side of figure 6) configured to define a number ("number of filter taps" in col. 5, line 2) of said video picture signals (Y and U,V inputs of fig. 6) to be buffered in said first memory circuit (Figure 2, num. 22 is a buffer located within figure 6, numeral 52 on the left hand side.) in response to said one or more first control signals (K_v is a first vertical scaling factor because it is predetermined as mentioned in col. 3, line 47, col. 6, lines 19,20 and from col. 6, line 58 to col. 7, line 2.).

Claim 12 is similar to claim 11, except for requiring another similar set of components which was addressed in claim 8.

Regarding 13, Makinowski et al. teaches the apparatus according to claim 1, wherein said second circuit (fig. 6, numerals 52 and 54 located on the right side of figure 6) controls an output rate (A phase offset is used to position chroma and luma components at the output at col. line. 8, lines 10-13) of said data signals (The outputs 52 and 54 on the left side of fig. 6.) from said first circuit (fig. 6, numerals 52 and 54 located on the left side of figure 6) in response to said first value ("order of vertical...scaling" at Makinowski et al., col. 6 line 62) and said second value ("order of... horizontal scaling" at Malinowski et al. , col. 6 line 62).

Claim 14 has been addressed in claim 11 above.

Regarding claim 15, Malinowski et al. teaches an apparatus (Fig. 6) for variably scaling video picture comprising:

a) means for (fig. 6, numerals 52 and 54 located on the left side of figure 6) generating one or more data signals (outputs of 52 and 54 on the left side of fig. 6) vertically scaled to a first value ("order of vertical...scaling" at Makinowski et al. , col. 6 line 62) in response to (i) said video picture signals (Y and U,V inputs of fig. 6) and (ii) one control signal (Malinowski et al., fig. 2, label "K1" is a control signal or "upscaling factor K (Malinowski et al., col. 3, line 47)" of the interpolator as shown in figure 2. The control signal is located within the interpolator of fig. 6, num. 52 on the right side of fig. 6.);

b) means for (fig. 6, numerals 52 and 54 located on the right side of fig. 6.) generating one or more output signals (Y and U,V outputs of fig. 6) horizontally scaled to a second value ("order of... horizontal scaling" at Malinowski et al. , col. 6 line 62 and 52 and 54 on the right side perform horizontal processing.) in response to (i) said one or more data signals (outputs of 52 and 54 on the left side of fig. 6) and (ii) said one or more control signals (Figure 6, numerals 52 and 54 on the right side of figure 6 have the same characteristics of numerals 52 and 54 located on the right side of figure 6 except for a horizontal scaling factor.), wherein said first value and said second value are independently selectable (Malinowski et al. states," the vertical and horizontal scaling factors may be independent (col. 7 lines 1,2).").

c) generating said one or more control signals (Upscaling factors, K_h and K_v mentioned in col. 6, lines 19,20.) configured to provide a number of states (Number of interpolations as mentioned in col. 4, lines 33-37 and col. 6, lines 19 and 20.)

The control signals K_h and K_v gives an indication of the number of iterations that corresponds to the way a video picture is shown. Thus, a single iteration shows the first state of a video picture.

Malinoski et al. does not teach the claimed state that is configured to allow multiple luma and chroma picture requests to follow in sequence. However, Malinoski et al. does teach of providing Y and UV signal components to the interpolator 52 of fig. 6 in col. 6, lines 60,61.

However, Shirota, in the field of endeavor of color video processing, teaches the limitation of a means (fig. 13, num. 70 is a control circuit) for generating one or more control signals (fig. 13, labels CT_3 to CT_6 , CT_A, CT_B , $CT_{,1,2,7,8}$) configured to provide a number of states (Y_{N3} to Y_{N6} of fig. 13 as mentioned in col. 20, lines 1-34.) configured to allow multiple luma and chroma picture requests ($(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$ for a luma picture request and $(SL_n)_c$ and $-(SL_n)_c$ for a chroma picture request of fig. 13 as mentioned in col. 19, lines 58-65 and col. 20, lines 36-39.) to follow in sequence ($(SL_{n+1})_y$, is requested first, $(SL_n)_y$,$(SL_n)_c$ and $-(SL_n)_c$, are requested second, and $(SL_{n-1})_y$, is requested last.)

The control circuit 70 generates output control signals, CT_3 to CT_6, CT_A, CT_B, $CT_{,1,2,7,8}$. The control signals allow one state from Y_{N3} to Y_{N6} to be outputted. Any one of the states are configured to allow the picture requests, $(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$ for a luma picture request and $(SL_n)_c$ and $-(SL_n)_c$ for a chroma picture request, to follow a sequence.

The sequence of the picture request is based on a delay time. The first picture requested at an initial time is $(SL_{n+1})_y$ which is outputted from num. 54 of fig. 13. The second request pictures at delay time τ_H that follow the first signal at the initial time are $(SL_n)_y$,$(SL_n)_c$ and $-(SL_n)_c$ which are outputted from 55 and 62 of fig. 13.The last picture request at delay time $2\tau_H$ is $(SL_{n-1})_y$ which is outputted from 56 of fig. 13, that follows after the second picture request at delay time τ_H as mentioned in col. 19, lines 52-68.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Malinowski et al.'s teaching of an interpolator 52 of fig. 6 with a scaling factor K as the claimed control signal with Shirota's teaching of a control circuit 70 and associated luma and chroma output control signals CT_A , CT_B , $CT_{1,2,7,8}$, CT_3 , CT_4, CT_5 , CT_6 of fig. 13 that correspond with the claimed control signal, because the luminance component or picture request, $(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$, will be free at all times of spatial deviation with respect to a line in col. 20, lines 31-33. Note that $(SL_n)_y$, $(SL_{n-1})_y$ and $(SL_{n+1})_y$ of Shirota are used to compute interpolation values as suggested by Malinowski's interpolator 52 of fig. 6.

Claim 16 has been addressed in claim 15.

Claim 17 has been addressed in claim 3.

Claim 18 has been addressed in claim 13.

Claim 19 has been addressed in claim 4.

12. Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) and in view of Shirota (US Patent 4,376,290 A) further in view of Iwase (US Patent 5,089,893 A).

Regarding claim 5, Malinowski et al. teaches a display line when some of a picture is not displayed. Makinowski et al. states,"...for a given set of input pixels, interpolations are generated so long as the accumulation of dx does not increment beyond the next integer pixel value (col. 4 line 31-33)."

However, Makinowski et al. does not teach the remaining portions of claim 20.

Iwase, in the field of endeavor of scaling at col. 2 lines 37-41, does teach the remaining portion of claims 20 and 5 of automatically resetting a display line address ("address AD" at col. 4, lines 30,31).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to use the teaching of Iwase of automatically resetting an address line with Makinowski et al. teaching of not interpolating beyond the next integer pixel value because Iwase's resetting of an address line provides proper information for a "respective subfilter" (Iwase, col. 4 lines 25-47).

Claim 20 has been addressed in claim 5.

13. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) in view of Shirota (US Patent 4,376,290 A) as applied to claim 1 above, and further in view of Fandrianto et al. (US Patent 5,982,459 A).

Regarding claim 10, Malinowski et al. teaches "scaling options available in a device incorporating the present invention that is used as a NTSC/PAL decoder...(col. 8, lines 40-42).", and accumulators at col. 3 line 66 for interpolation and col. 5 lines 1,2 for decimation).

Makinowski et al. does not teach the use of a single-chip MPEG-2 decoder as required of claim 10.

However, Fandrianto et al., in the field of endeavor of interpolation (col. 3 line. 18), does teach a single-chip (fig. 1, num. 110: VCP) MPEG-2 decoder (Fandrianto et al. at col. 3 lines 9-11).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to use Fandrianto et al.'s VCP single-chip with MPEG-2 decoding to modify Makinowski et al. accumulation calculations of interpolation and decimation because Fandrianto et al.'s VCP single-chip is capable of decoding multiple standard video formats MPEG 1 and MPEG 2 per a committee that propagates video standards (Fandrianto et al., col. line. 3, lines 11-15).

14. Claims 21,22 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) in view of Shirota (US Patent 4,376,290 A) as applied to claim 1 above, and further in view of Ozcelik et al. (US Patent 6,078,616 A).

Regarding claim 21 Malinowski et al. does not teach a finite state machine with the claimed states. However, Malinowski does suggest various processing states "State 0-5" of a filter for processing video signals as mentioned from col. 5, line 30 to col. 6, line 12.

Ozcelik et al. does teach claim 21 of an apparatus, wherein a finite state machine (fig. 6) comprises an idle after chroma state (fig. 6, num. 620 is a waiting state after a previous chroma state 614.) configured to move (via arrow direction of numerals 622,626 and 628) to a luma state (Fig. 6, num. 624).

Regarding claim 22 Ozcelik et al. does teach an apparatus wherein a finite state machine (fig. 6) comprises an idle after luma state (fig. 6, num. 620 is a waiting state after a previous luma state 606.) configured to move (via arrow direction of numerals 622,626 and 628) to a luma state (Fig. 6, num. 624).

Regarding claim 23 Ozcelik et al. does teach an apparatus, wherein a finite state Machine (fig. 6) provides (i) an idle after chroma state (fig. 6, num. 620 is a waiting state after a previous chroma state 614.) configured to move (via numerals 622,626,628,624,630) to a chroma state (fig. 6, num. 632 is a chroma state) in response to a first predetermined condition (output of 618 of fig. 6 is a previous process.) and (ii) an idle after luma state (fig. 6, num. 606 is a waiting state for luma data) configured to move to a luma state (fig. 6, num. 612) in response to a second predetermined condition (State 606 moves to 612 when 606 receives luma reference data.)

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the filter states of Malinowski et al. with Ozcelik et al. state machine of figure 6, which is also shown as 502 coupled to a filter 504 as shown in fig. 5, because Ozcelik et al.'s state machine constructs a macroblock that effectively conceals an error in a data steam as mentioned in col. 4, lines 18-20 and col. 7, lines 57-61.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario-Vasquez whose telephone number is 703-305-5431. The examiner can normally be reached on 9-5.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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